

[sequence] a sequential column address access.

D3  
end  
11  
21. (Once Amended) A storage device, as in Claim <sup>10</sup>20, wherein the sequence column address access is selected from a group consisting of an interleaved column address access and a linear column address access.

Please add the following new claims:

D4  
cont  
15  
62. (New) A storage device comprising:  
control logic for selecting between a patternless addressing scheme and a patterned addressing scheme;  
a counter; and  
switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected, wherein the first pathway and the second pathway are coupled to a temporary storage device for providing at least one external address to the switching circuitry, and wherein the counter is coupled to the temporary storage device to receive a selected portion of the external address for generating an internal address.

16  
63. (New) The storage device of Claim <sup>15</sup>62, wherein the internal address is provided to the temporary storage device through the switching circuitry

17  
64. (New) The storage device of Claim <sup>15</sup>62, wherein the patternless addressing scheme provides a pipelined extended data out pattern.

18  
65. (New) A storage device comprising:  
control logic for selecting between a patternless addressing scheme and a patterned addressing scheme; and  
switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme

is selected, wherein the patternless addressing scheme provides a pipelined extended data out pattern.

<sup>19</sup>  
66. (New) The storage device of Claim <sup>18</sup>65, wherein the patterned addressing scheme provides a burst extended data out pattern.

<sup>20</sup>  
67. (New) The storage device of Claim <sup>18</sup>65, wherein the switching circuitry includes at least one multiplexed device.

<sup>21</sup>  
68. (New) A storage device comprising:  
control logic for selecting between a patternless addressing scheme and a patterned addressing scheme; and  
switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected, wherein the patterned addressing scheme provides a burst extended data out pattern.

<sup>22</sup>  
69. (New) The storage device of Claim <sup>21</sup>68, wherein the switching circuitry includes at least one multiplexed device.

<sup>23</sup>  
70. (New) A memory device, comprising:  
a memory array operable in a burst mode of operation or a pipelined mode of operation;  
control logic for selecting between the burst mode of operation or the pipelined mode of operation; and

switching circuitry for switching between a first, burst data pathway and a second, pipeline data pathway depending on which of the burst or pipelined modes of operation is selected, wherein the first pathway and the second pathway are coupled to a temporary storage device for providing at least one external address to the switching circuitry.

<sup>24</sup>  
71. (New) The memory device of Claim <sup>23</sup>70, further comprising a counter coupled to the temporary storage device to receive a selected portion of the external address for generating an